PATENT ABSTRACTS OF JAPAN

(11)Publication number : **09-161472**

(43)Date of publication of application : **20.06.1997**

(51)Int.Cl. **G11C 7/00**

G06F 1/06

G11C 11/407

(21)Application number : **07-324248**

(22)Date of filing : **13.12.1995**

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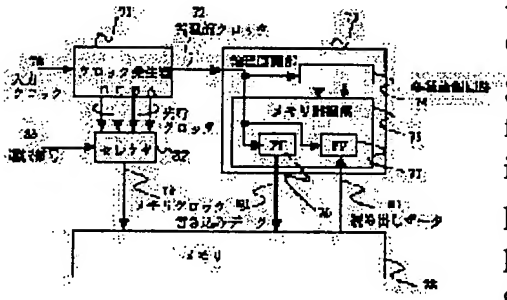
(54) MEMORY CONTROL METHOD



(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a sure optimum, and stable access timing margin.

SOLUTION: A PLL(Phase Locked Loop) including a ring oscillator type voltage controlled oscillator is used for a clock generator 71 of an LSI, a logic part clock 72 for the logic circuit part is generated from an input clock 70, and at the same time, a plurality of advance clocks with a different phase from that of the logic part clock 72 are generated. Then, a memory clock 79 with an optimum phase is selected, a write data which is outputted in synchronization with the logic part clock 72 is written to a memory 78 by the memory clock 79, and read data 81 which are outputted in synchronization with the memory clock 79 are read from the memory 78 by the logic part clock 72.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]About the control method of semiconductor memory, this invention relates to the memory control method which enabled it to obtain the timing margin of transmission of data certainly, also when a high-speed operation clock is used especially.

[0002]

[Description of the Prior Art]Although the large scale integration circuit LSI (Large Scale Integration) generally operates with a clock, In that case, there are a method of using the clock inputted from the outside as it is as a feeding method of the clock to be used, and a method of multiplying the clock inputted from the outside, and generating and using a high-speed logic clock. Especially since the latter method can be changed and supplied to the optimal frequency for the operating characteristic of LSI which uses the clock frequency inputted from the outside, it is useful, and it is used widely.

[0003]Next, the example of the conventional circuitry at the time of applying the latter method to memory control is explained using drawing 11. As for a clock generation circuit and 113, in the figure, a memory control part and 118 are memories a logic circuit section and 115 111. The input clock 110 from the outside is multiplying-ized with the clock generation machine 111, and turns into the Boolean part clock 112. The Boolean part clock 112 obtained with the clock generation machine 111 is given to the logic circuit section 113, and it is used as a clock of the various logic circuits 114 in the inside of the logic circuit section 113, and also it is supplied to the memory control part 115 and the memory 118. Drawing 11 showed the clock supplied to the memory 118 as the memory clock 119. FF116 and FF117 inside the memory control part 115 mean a flip flop group, and they are used, respectively in order to hold the write data 120 to the memory 118, and the read data 121 from the memory 118. The Boolean part clock 112 mentioned above also as a clock of these flip flop group FF116 and FF117 is used.

[0004]Drawing 12 is a time chart which shows the access timing of the memory 118. Although drawing 12 showed writing and read-out repeatedly as a series of continuous operations, writing and read-out shall be actually made to separate timing. This example shows the case where multiplied the input clock 110 twice and it is considered as the Boolean part clock 112 and the memory clock 119. A synchronous memory shall be used as the memory 118. In the synchronous memory 118, writing of data and read-out are altogether performed synchronizing with a clock. The write data 120 is outputted from the memory control part 115 by write data output timing (A). It is outputted after delay by a

flip-flop, and is written in the memory 118 by synchronous memory writing timing (B). If a read-out command (based on the control signal which is not illustrated) is outputted to read data demand timing (C), the read data 121 will be outputted after the access time of the memory 118, and it will be read by the memory control part 115 by read data read timing (D).

[0005]

[Problem(s) to be Solved by the Invention]In the above-mentioned conventional technology, when an operation clock was high-speed, it became clear in the data transfer that timing margins ran short. That is, it may consist [whether the cycle of a clock is comparable as the access time of a memory, and] of it. In this case, it turned out that the reading margin (F) shown in drawing 12 is insufficient, and malfunctions. Although a part for one clock is held from write data output timing, if the phase of a memory clock is delayed, the write-in margin (E) shown in drawing 12 will be insufficient for write data, and it will malfunction. Especially when the memory 118 is in the exterior of LSI, malfunction by shortage of a timing margin breaks out easily. The purpose of this invention cancels the fault of the above-mentioned conventional technology, and there is in providing the memory control method that the timing margin of access can be obtained certainly. Other purposes of this invention are to provide the memory control method that it can make it possible to set up the timing margin of access the optimal. Other purposes of this invention are to provide the memory control method that the timing margin of stable access can be obtained, also to change of temperature and power supply voltage.

[0006]

[Means for Solving the Problem]To achieve the above objects, a memory control method of this invention, It is a phase-locked loop () to the clock generation machine 11. [Phase-Locked Loop and] the following -- only -- PLL -- saying -- it using, and the Boolean part clock 12 for the logic circuit section 13, [generate and] The memory clock 19 with which the Boolean part clock 12 furthermore differs from a phase from the PLL is generated, The read data 21 which writes the write data 20 outputted synchronizing with the Boolean part clock 12 in the memory 18 with the memory clock 19, and is outputted synchronizing with the memory clock 19 is incorporated into the memory control part 15 with the Boolean part clock 12 (refer to drawing 1 and drawing 2). Two or more precedence clocks (A, B, C, D) with which the Boolean part clock 72 differs from a phase from the above-mentioned PLL are generated, one of them is chosen, and it is considered as the memory clock 79 (refer to drawing 7 and drawing 8). A clock is outputted from a predetermined tap of a ring oscillator, using a ring oscillator as a voltage controlled oscillator (:Voltage Controlled Oscillator called the following and

VCO) in PLL, Several clocks with which phases differ are obtained, one of them is chosen, and it is considered as a memory clock (drawing 9, ten references).
[0007]
[Embodiment of the Invention]In this invention, a clock generation machine is constituted from PLL, the memory clock with which the Boolean part clock differs from a phase from this PLL is generated, a clock with an early phase is used as a memory clock, and a clock with a late phase is used as a Boolean part clock. Thereby, a write-in margin and a reading margin can be raised. Since two or more Boolean part clocks and clocks with which phases differ can be generated, arbitrary one out of them can be chosen from PLL and it can be considered as a memory clock, the timing margin of access can be set up the optimal. Since the ring oscillator which constitutes PLL can generate several clocks with which phases (time delay) differ correctly according to the number of stages even if it changes temperature and power supply voltage, it can obtain the timing margin of stable access.
[0008]
[Example]Hereafter, the 1st example of this invention is described using drawing 1 - drawing 6. In drawing 1, 11 is a memory control part to which a clock generation machine and 13 perform the logic circuit section in LSI, 14 performs various logic circuits, and 15 performs various control for memory access. 18 is a synchronous memory controlled by the memory control part 15, for example, is taken as external memory. The clock generation machine 11 generates the Boolean part clock 12 and the memory clock 19 from the input clock 10 from the outside. The Boolean part clock 12 is used as a clock of the various logic circuits 14 in the inside of the logic circuit section 13, and also it is supplied to the memory control part 15. FF16 and FF17 inside the memory control part 15 mean a flip flop group, and they are used, respectively in order to hold the write data 20 to the memory 18, and the read data 21 from the memory 18. The Boolean part clock 12 mentioned above also as a clock of these flip flop group FF16 and FF17 is used. This example differs from the conventional example which the method of generating of a memory clock with a clock generation machine showed to drawing 11.
[0009]The operation timing of the circuit of drawing 1 is shown in drawing 2. Although writing and read-out are repeatedly shown as a series of continuous operations like drawing 12 also in drawing 2, writing and read-out are actually made to separate timing. Suppose that it is the Boolean part clock 12 and the memory clock 19 twice the frequency of the input clock 10 in this example. The memory clock 19 has a phase earlier than the Boolean part clock 12. Since the memory 18 is a synchronous memory, writing and read-out of data are altogether performed synchronizing with a clock.

[0010]Now, the write data 20 is outputted from the memory control part 15 by write data output timing (a). It is outputted after delay of FF16 and written in the memory 18 by synchronous memory writing timing (b). The phase of the memory clock 19 writes in only an early part as compared with the phase of the Boolean part clock 12, and a margin improves. If a read-out command (based on the control signal of the address etc. which are not illustrated) is outputted to read data demand timing (c) synchronizing with the Boolean part clock 12, This command is read by the memory 18 with the following memory clock (d), and the read data 21 is outputted after the access time (e) of the memory 18, and it is read by the memory control part 15 by the read data read timing (f) in sync with the Boolean part clock 12. Since the read data 21 is early outputted for the phase of the memory clock 19 only an early part also in this case as compared with the Boolean part clock 12, a reading margin can be improved. A timing margin can be obtained certainly as mentioned above. In the above-mentioned example, it is a case where CAS latency of the memory 18 is set to 1.

[0011]Drawing 3 is an example of an internal configuration of the clock generation machine 11 in the example of this invention shown in drawing 1. The clock generation machine 11 in this example is constituted by PLL (phase-locked loop) known well. Operation of PLL is stated to the Yanagisawa **** "PLL (phase-locked loop) application circuit" (September 20, Showa 52 synthesis electronic publishing company issue) in detail, for example. The clock generation machine 11 constituted from PLL comprises the phase comparator 31 (PD), the voltage controlled oscillator 36 (VCO:Voltage Controlled Oscillator), the counting-down circuit 37 (CNT), etc., as shown in drawing 3.

[0012]The phase comparator 31 (PD) is a circuit which makes a DOWN output a low level, while the phase of the Boolean part output clock 38 after the input clock 10 and dividing is compared, UP output is made into a low level when latter one is late, and latter one is progressing conversely. Drawing 4 is an example of concrete composition of the phase comparator 31 (PD).

Since it is detailed in said literature about operation, it explains briefly.

The phase comparator 31 (PD) has circuitry shown, for example in drawing 4.

It is a circuit which generates the UP signal and DOWN signal corresponding to phase contrast of the input clock 10 and the logic clock 38 after dividing.

In this circuit, when the input clock 10 is advancing from the logic clock 38 after dividing, only the advanced phase contrast outputs the UP signal set to a low level, Conversely, when the input clock 10 is behind the logic clock 38 after dividing, only the width of the phase which is behind outputs the DOWN signal set to a low level.

[0013]The voltage controlled oscillator 36 (VCO:Voltage Controlled Oscillator), The signal (CP) decided by the output (UP output and a DOWN output) of the

phase comparator 31 (PD) mentioned above is considered as an input, Oscillating frequency is changed with the value of the CP (refer to drawing 5), and the phase of the Boolean part clock 12 which is the output is carried out early, or it is made late, and the phase of the input clock 10 is made to approach (the phase contrast of the input clock 10 and the Boolean part clock 12 is decreased).

[0014]Next, the operation is explained still in detail. If UP output serves as a low level (the phase of the Boolean part clock is behind), the capacity 35 is charged via the resistance 34 and the p channel MOS transistor 32, and CP voltage used as the control voltage of the voltage controlled oscillator 36 is increased. [the p channel MOS transistor 32] If CP voltage goes up, since the oscillating frequency of the voltage controlled oscillator 36 (VCO) becomes high, in the phase of the Boolean part clock 12 after dividing, the phase of the Boolean part clock 12 will come to approach the phase of the input clock 10 as a result early. On the contrary, if a DOWN output serves as a low level (the phase of the Boolean part clock is progressing), the signal will become high-level via an inverter, and will be impressed to the gate of the n channel MOS transistor 33. Since the n channel MOS transistor 33 with which the high-level signal was impressed to the gate is turned on, the capacity 35 is discharged via the resistance 34 and the n channel MOS transistor 33, and drops CP voltage used as the control voltage of the voltage controlled oscillator 36 (VCO). If CP voltage falls, since the oscillating frequency of the voltage controlled oscillator 36 (VCO) becomes low, the phase of the Boolean part clock 12 after dividing will become late, and the phase of the Boolean part clock 12 will come to approach the phase of the input clock 10 as a result. In this example, dividing of the counting-down circuit 37 (CNT) shall be carried out to the frequency of 1/2. The memory clock 19 has also been obtained from the voltage controlled oscillator 36 (VCO) besides the Boolean part clock 12.

[0015]Drawing 5 is an example of concrete composition of the voltage controlled oscillator 36 (VCO) of drawing 3. In the figure, M1-M28 are MOS transistors. The p channel MOS transistor M1, M2, M5, M9, M13, M17, M21, and M25 constitute a current mirror, The n channel MOS transistor M4, M8, M12, M16, M20, and M24 constitute the current mirror, and the same current can be sent by designing in the respectively same shape. The p channel MOS transistor M6, the n channel MOS transistor M7 and the p channel MOS transistor M10, the n channel MOS transistor M11 and the p channel MOS transistor M14, and the n channel MOS transistor M15, The p channel MOS transistor M18, the n channel MOS transistor M19 and the p channel MOS transistor M22, and the n channel MOS transistor M23, The ring oscillator is constituted by forming an inverter, respectively and connecting those inputs and outputs to ring shape.

[0016]The p channel MOS transistor M25, the n channel MOS transistor M26 and the p channel MOS transistor M27, and the n channel MOS transistor M28 also

constitute the inverter, It is working as a buffer for obtaining the Boolean part clock 12 and the memory clock 19, respectively. Among the figure, AVCC and AGND are the power supplies of voltage controlled oscillator 36 (VCO) exclusive use, in order to control noise, with the power supply of the logic circuit section of the same LSI, dissociate and are provided. In the p type semiconductor substrate, since it is easy to receive noise from a substrate, the board power supply ASUB dissociates and the n channel MOS transistor is provided.

[0017]If the voltage of CP goes up, in order that resistance of the n channel MOS transistor M3 may decrease, the p channel MOS transistor M2 and M -- while reducing the gate voltage of 5, M9, M13, M17, and M21 -- the n channel MOS transistor M4 and M, in order to raise the gate voltage of 8, M12, M16, M20, and M24, The current which flows into a ring oscillator increases, the charge and discharge time of the capacity (not shown) of each stage of a ring oscillator becomes short, and oscillating frequency goes up. On the contrary, since resistance of the n channel MOS transistor M3 will increase if the voltage of CP falls, the p channel MOS transistor M2 and M -- while raising the gate voltage of 5, M9, M13, M17, and M21 -- the n channel MOS transistor M4 and M, in order to reduce the gate voltage of 8, M12, M16, M20, and M24, The current which flows into a ring oscillator decreases, the charge and discharge time of the capacity (not shown) of each stage of a ring oscillator becomes long, and oscillating frequency falls. The Boolean part clock 12 is obtained from the output of the p channel MOS transistor M22 and the n channel MOS transistor M23, Since the memory clock 19 is obtained from the output of the p channel MOS transistor M14 and the n channel MOS transistor M15, the memory clock 19 becomes what has an early phase by two stages of a ring oscillator from the Boolean part clock 12.

[0018]Next, it explains in more detail about a ring oscillator using a wave form chart of operation. Drawing 6 shows change of the node voltage N1 of each stage in five steps of ring oscillators shown in drawing 5, N2, N3, N4, and N5. If the node voltage N1 changes high-level from a low level, the node voltage N2 will change from high level to a low level. Thereby, the node voltage N3 changes high-level from a low level. Since the same transition spreads one after another and is fed back to ring shape, each node (tap) oscillates. Approximately, high level to a transition travelling period high-level from a low level and a low-level transition travelling period are equal, and set this to Tpd. An oscillation cycle serves as 10Tpd so that drawing 6 may show. Generally, if the number of stages of a ring oscillator is set to N, an oscillation cycle will serve as 2 NxTpd. In drawing 3, when setting frequency of the input clock 10 to Fin, making the division ratio of the counting-down circuit 37 (CNT) into A/B and PLL locks, it turns out that there is the following relation (when a phase is in a stationary state).

Fin ={1/(2 NxTpd)} xA/B, therefore Tpd={1/(2NFin)} xA/B [0019]As explained above, the phase delay time for one step of a ring oscillator can be uniquely become final and conclusive with the input frequency Fin and the number of stages of PLL. In drawing 5, since the Boolean part clock 12 and the memory clock 19 are outputted from the tap from which a ring oscillator differs by two steps, as for the memory clock 19, a phase becomes early from the Boolean part clock 12 only 2 Tpd. Oscillation cycle 10Tpd of a ring oscillator is not influenced even if it changes temperature and power supply voltage. As explained above, according to the number of stages of a ring oscillator, several clocks with which phases (time delay) differ correctly can be obtained, and it becomes possible by making these into the Boolean part clock and a memory clock to raise the write-in margin of a memory, and a reading margin. Although drawing 5 and drawing 6 showed the example of a five-step ring oscillator, if a ring oscillator with many number of stageses is used, phase contrast 2Tpd of the Boolean part clock 12 and the memory clock 19 can be made small, and fine adjustment will become possible.

[0020]Drawing 7 - drawing 9 explain the (2nd example), next the 2nd example of this invention. Drawing 7 is the same as the 1st example shown in drawing 1 except the generation method of a clock generation machine and a memory clock. In drawing 7, 70 an input clock and 71 a clock generation machine and 72 The Boolean part clock, 73 -- a logic circuit section and 74 -- various logic circuits and 75 -- a memory control part, and 76 and 77 -- as for write data and 81, a memory and 79 are [a selector and 83] selection signals read data and 82 a memory clock and 80 a flip flop group and 78. In this example, two or more (this example four, A, B, C, and D) clocks (precedence clock) whose phase is earlier than the Boolean part clock 72 are obtained from the clock generation machine 71. Two or more of these precedence clocks are inputted into the selector 82, and after they choose the clock of the optimal phase with the selection signal 83, they are used as the memory clock 79.

[0021]The operation timing of the circuitry of drawing 7 is shown in drawing 8. In this example, both the Boolean part clock 72 and the memory clock 79 suppose that it is twice the frequency of an input clock. The four precedence clocks A, B, and C and D presuppose that it is in phase relation which was illustrated. Even if it precedes phase relation with the Boolean part clock 72, it can be rubbed as being delayed, and can be made, but it is made to call it a precedence clock on the relation of explanation, as mentioned above. In this example, these one is chosen and it is considered as the memory clock 79. The example of drawing 8 shows the case where the precedence clock B is chosen. The delay from the precedence clock B selected here to memory clock 79 output is based on the selector 82. The optimal lead time needs to decide that a write-in margin and a

reading margin are acquired properly. Since it is dependent on the mounted state of the shape of a printed circuit board of LSI and the synchronous memory which are considered to be an object now, after mounting, these margins are dramatically effective and it is useful that the optimal precedence clock can be chosen. The circuit which generates such two or more precedence clocks is realizable by the same PLL as drawing 3. The difference from the 1st example is in voltage controlled oscillator VCO in the clock generation machine 71.

[0022]The voltage controlled oscillator (VCO) of this example is shown in drawing 9. What is necessary is just to output an oscillation output from two or more taps of a ring oscillator, as shown in this figure. The p channel MOS transistor M25, the n channel MOS transistor M26 and the p channel MOS transistor M27, the n channel MOS transistor M28 and the p channel MOS transistor M29, and the n channel MOS transistor M30, By making the same shape of each inverter buffer of the p channel MOS transistor M31, the n channel MOS transistor M32 and the p channel MOS transistor M33, and the n channel MOS transistor M34, Since the capacity of each tap of a ring oscillator can be designed equally, phase contrast between the Boolean part clock 72, the precedence clock A, B, and C, and each of D can be made equal, and the optimal precedence clock can be obtained from the precedence clock A, B, and C and either of the D.

[0023]The (3rd example), next the 3rd example of this invention are described using drawing 10. This example realizes the voltage controlled oscillator (VCO) of the 2nd above-mentioned example by another circuit. In this example. Between each stage of a ring oscillator. A transfer gate. the p channel MOS transistor M35, the n channel MOS transistor M36 and the p channel MOS transistor M37, the n channel MOS transistor M38 and the p channel MOS transistor M39, and the n channel MOS transistor M40. The resistance depended for consisting of the p channel MOS transistor M41, the n channel MOS transistor M42 and the p channel MOS transistor M43, and the n channel MOS transistor M44 is inserted. In this composition, the gate voltage of the MOS transistor which constitutes a transfer gate, As drawing 5 explained, since it is controlled by voltage of CP via the p channel MOS transistor M1, M2 and the n channel MOS transistor M3, and M4, the resistance by a transfer gate turns into a variable resistor depending on the pressure value of CP. If it resists small by raising CP, oscillating frequency will become large, and conversely, CP will be reduced, and if resistance by a transfer gate is enlarged, oscillating frequency will become small and will perform the same operation as drawing 9. Although this example is shown as composition which transformed the 2nd example (drawing 9), it cannot be overemphasized that it can apply also as a modification of the 1st example (drawing 5).

[0024]
[Effect of the Invention]According to this invention, when accessing a memory with a high-speed clock, the timing margin of transmission of data can be obtained certainly. A timing margin can be set up the optimal. A stable timing margin can be obtained also to change of temperature and power supply voltage.

CLAIMS

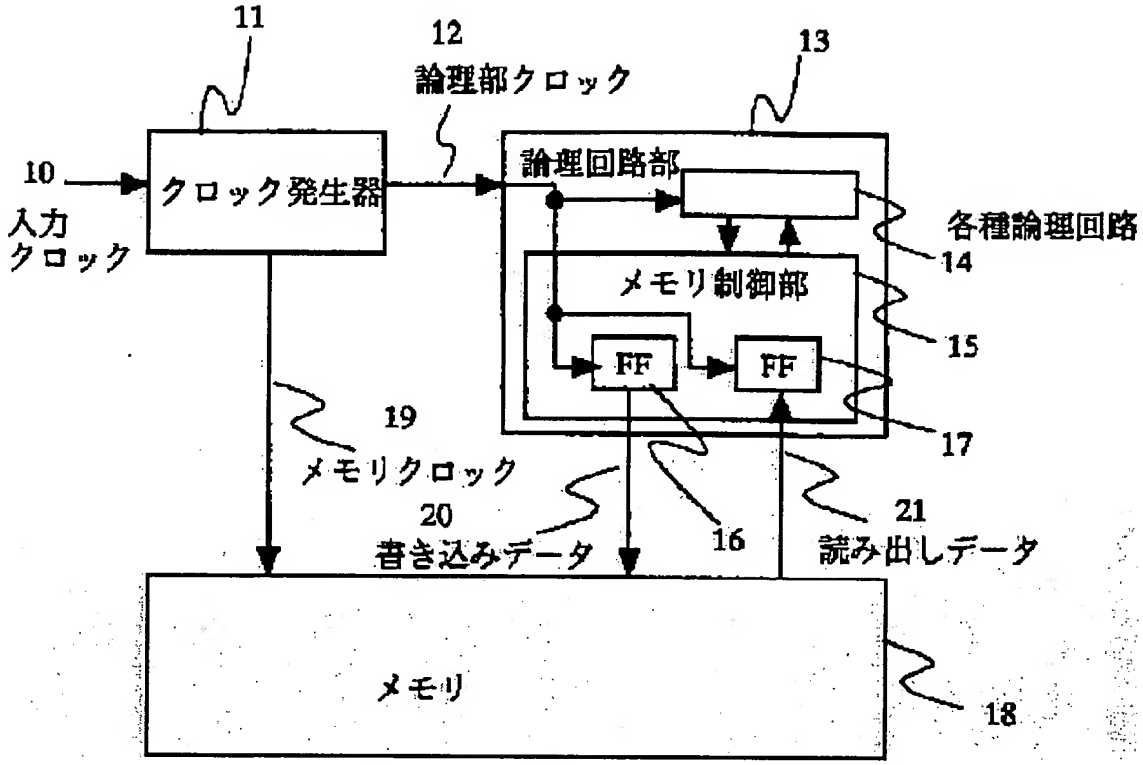
[Claim(s)]
[Claim 1]A memory.
A logic circuit section containing a memory control part which incorporates read data from this memory while giving write data at least to this memory.
A clock generation machine using a phase-locked loop.
Are the above the memory control method which it had, and with said clock generation machine or its output. The 1st clock, this 1st clock, and the 2nd clock with which phases differ are generated from an input clock, Said 1st clock is supplied to said logic circuit section, said 2nd clock is supplied to said memory, a memory control part in said logic circuit is operated with said 1st clock, and said memory is operated with said 2nd clock.

[Claim 2]A memory control method being what said 2nd clock generates several clocks with which said 1st clock differs from a phase, and produced from two or more this generated clocks by choosing one clock in a memory control method according to claim 1.
[Claim 3]In a memory control method according to claim 1 or 2, a voltage controlled oscillator which is a component of said phase-locked loop is constituted using a ring oscillator, A memory control method obtaining said 1st clock and the 2nd clock from a tap output signal of this ring oscillator.

[Brief Description of the Drawings]
[Drawing 1]It is a lineblock diagram of the 1st example of this invention.
[Drawing 2]It is an operation timing figure of the 1st example of this invention.
[Drawing 3]It is a lineblock diagram of the clock generation machine of the 1st example of this invention.
[Drawing 4]It is a lineblock diagram of the phase comparator of the 1st example of this invention.

[Drawing 5]It is a lineblock diagram of the voltage controlled oscillator of the 1st example of this invention.
[Drawing 6]It is an explanatory view of the voltage controlled oscillator of the 1st example of this invention of operation.
[Drawing 7]It is a lineblock diagram of the 2nd example of this invention.
[Drawing 8]It is an operation timing figure of the 2nd example of this invention.
[Drawing 9]It is a lineblock diagram of the voltage controlled oscillator of the 2nd example of this invention.
[Drawing 10]It is a lineblock diagram of the voltage controlled oscillator of the 3rd example of this invention.
[Drawing 11]It is a lineblock diagram of conventional technology.
[Drawing 12]It is an operation timing figure of conventional technology.

10, 70,110: Input clock,
11, 71,111: Clock generation machine,
12, 72,112: Boolean part clock,
13, 73,113: Logic circuit section,
14, 74,114: Various logic circuits,
15, 75,115: Memory control part,
16, 17, 76, 77,116,117: Flip flop group
18, 78,118: Memory (synchronous memory),
19, 79,119: Memory clock,
20, 80,120: Write data,
21, 81,121: Read data,
31: Phase comparator (PD),
32: P channel MOS transistor,
33: N channel MOS transistor,
34: Resistance,
35: Capacity,
36: Voltage controlled oscillator (VCO:Voltage Controlled Oscillator)
37: Counting-down circuit (CNT)
38: The Boolean part clock after dividing,
82: Selector,
83: Selection signal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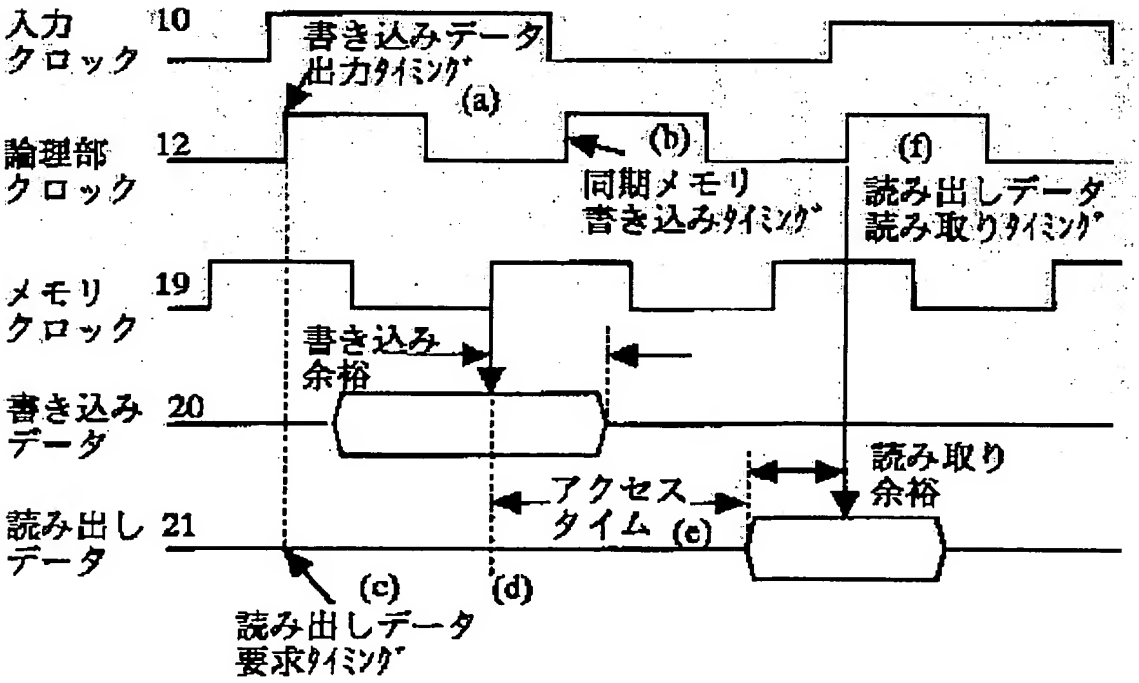
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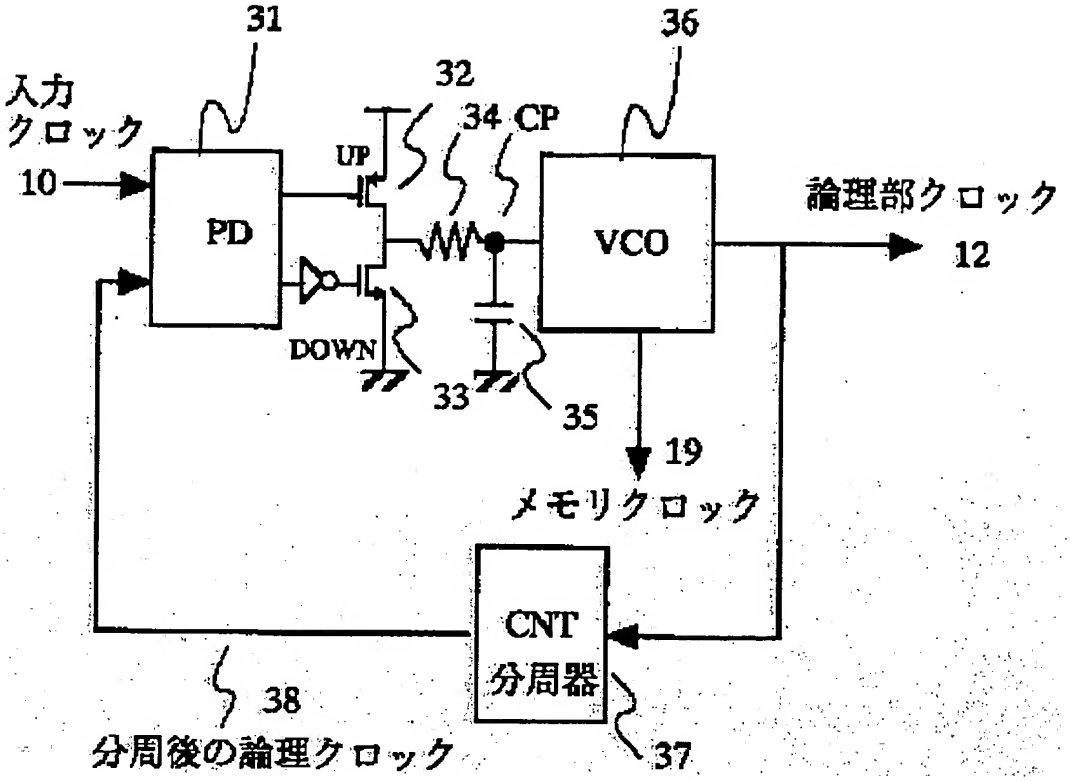
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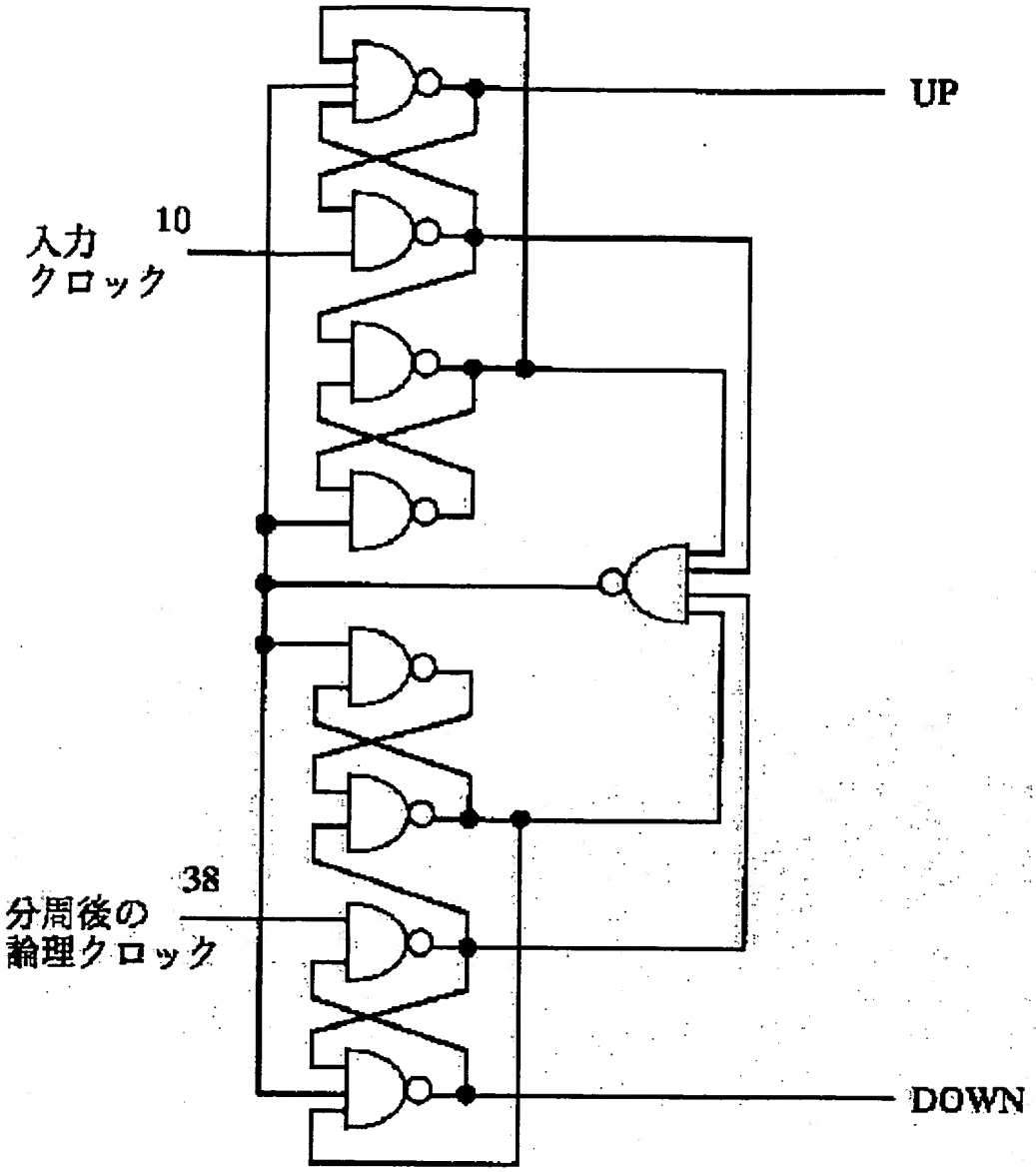
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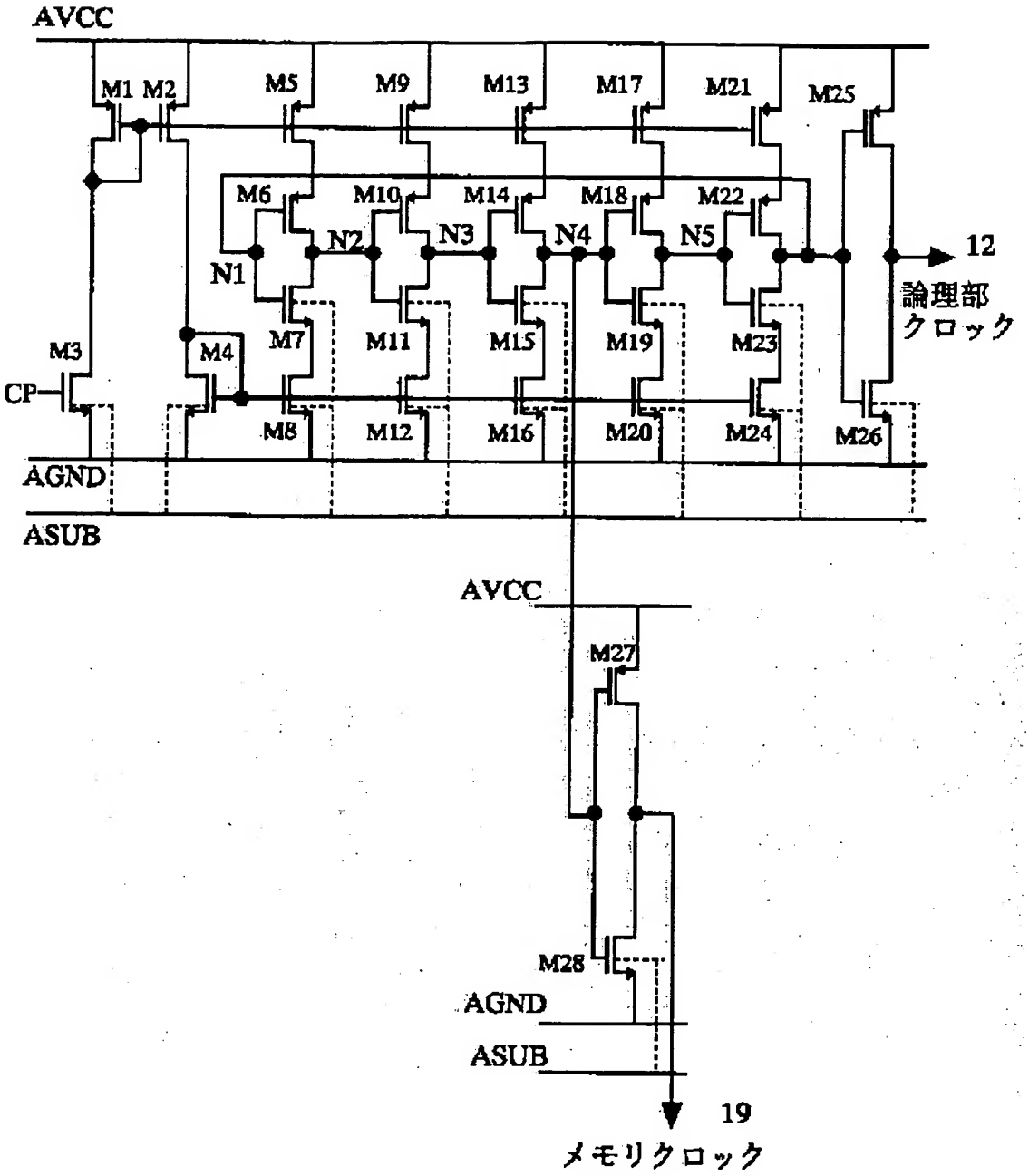
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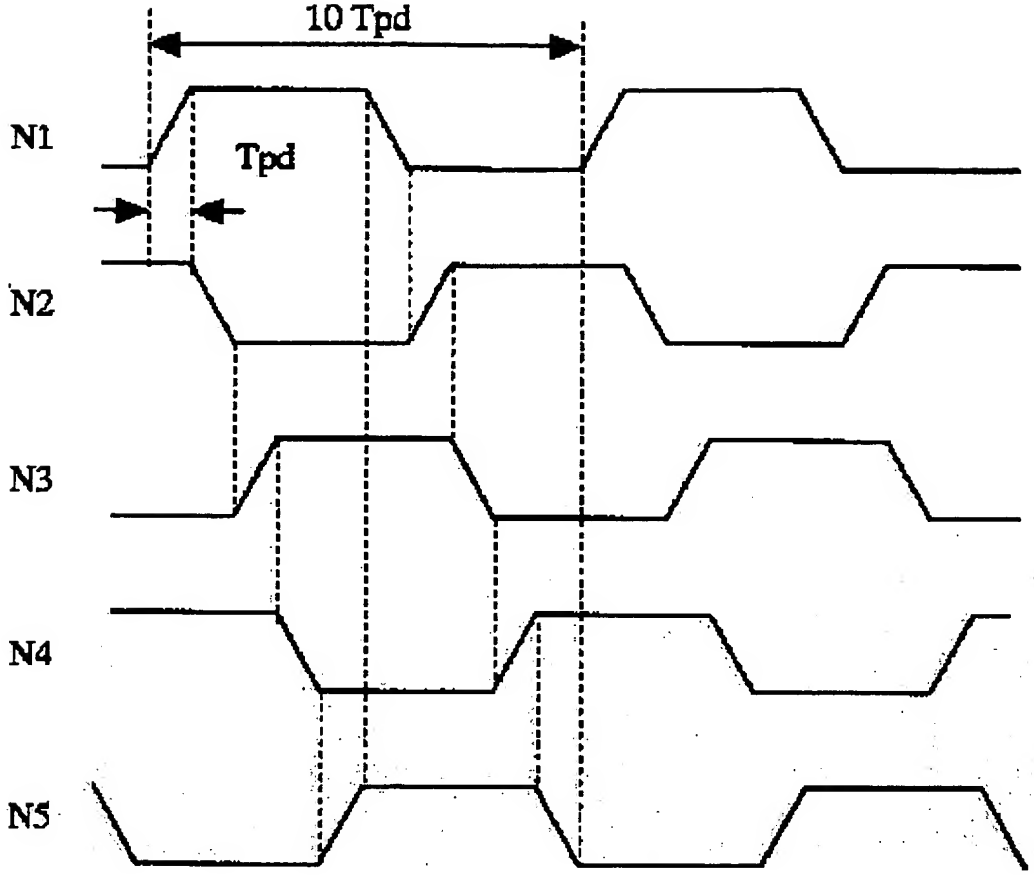
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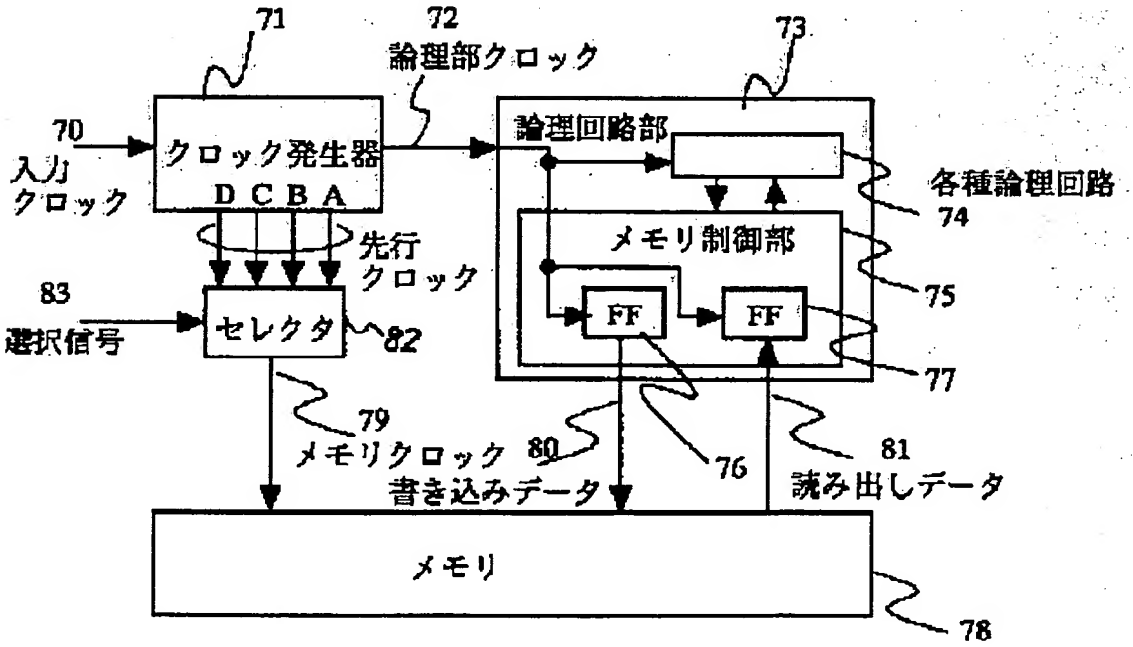
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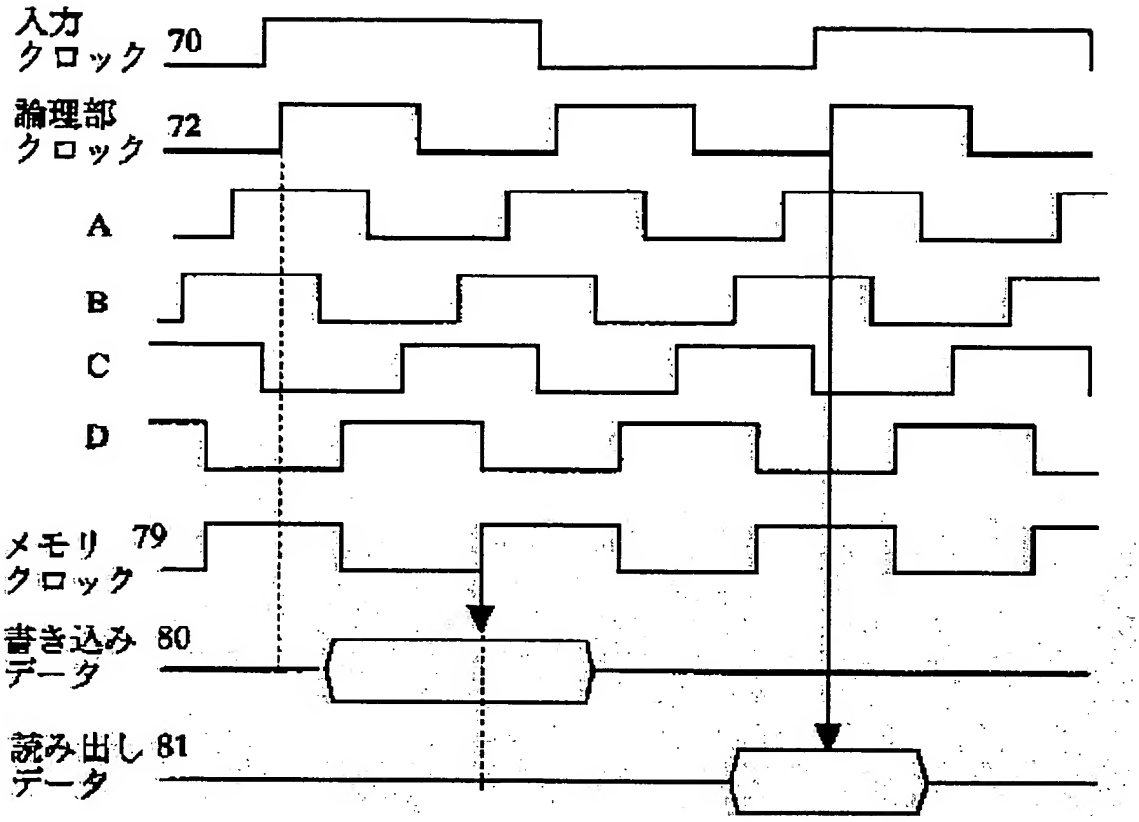
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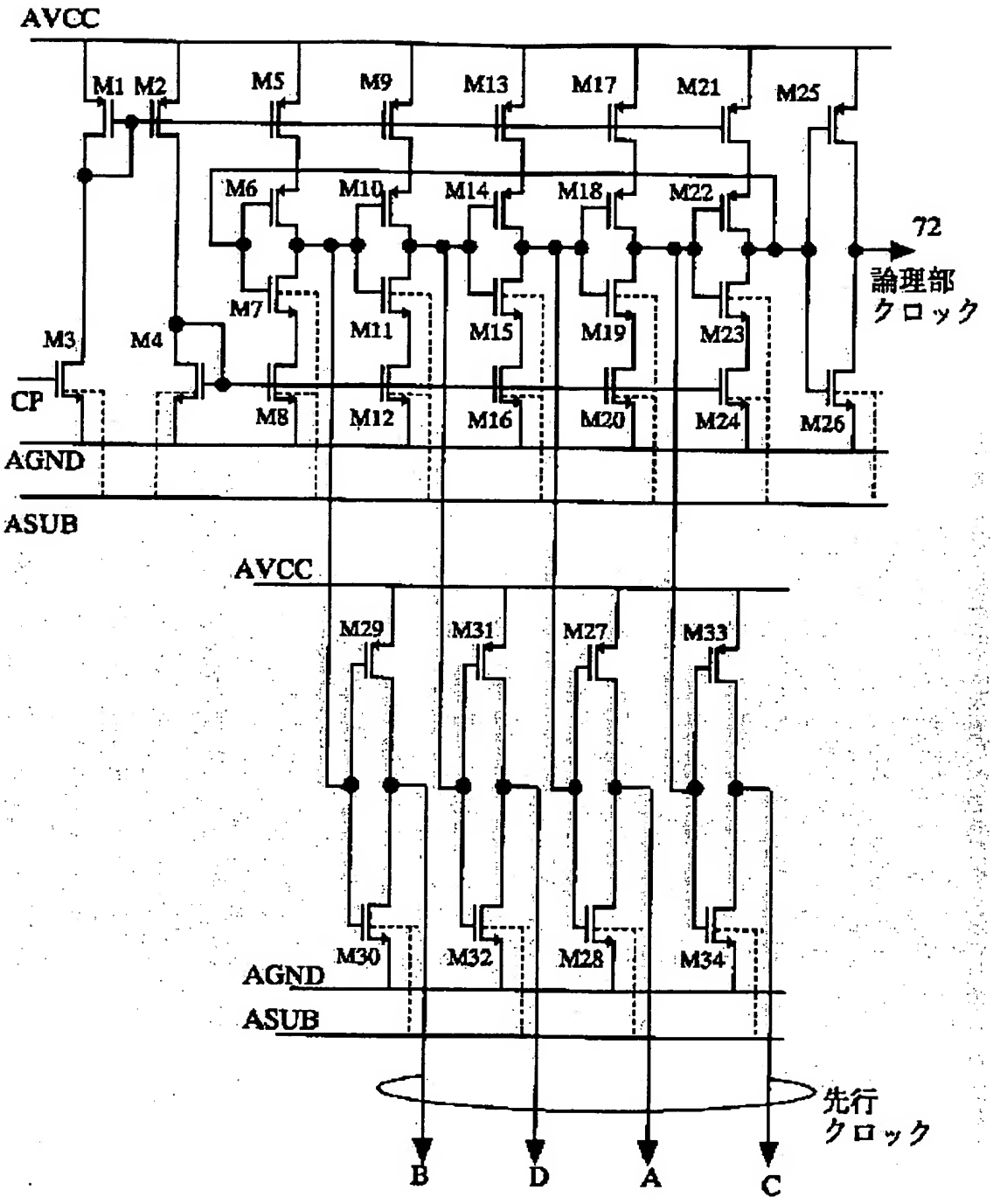
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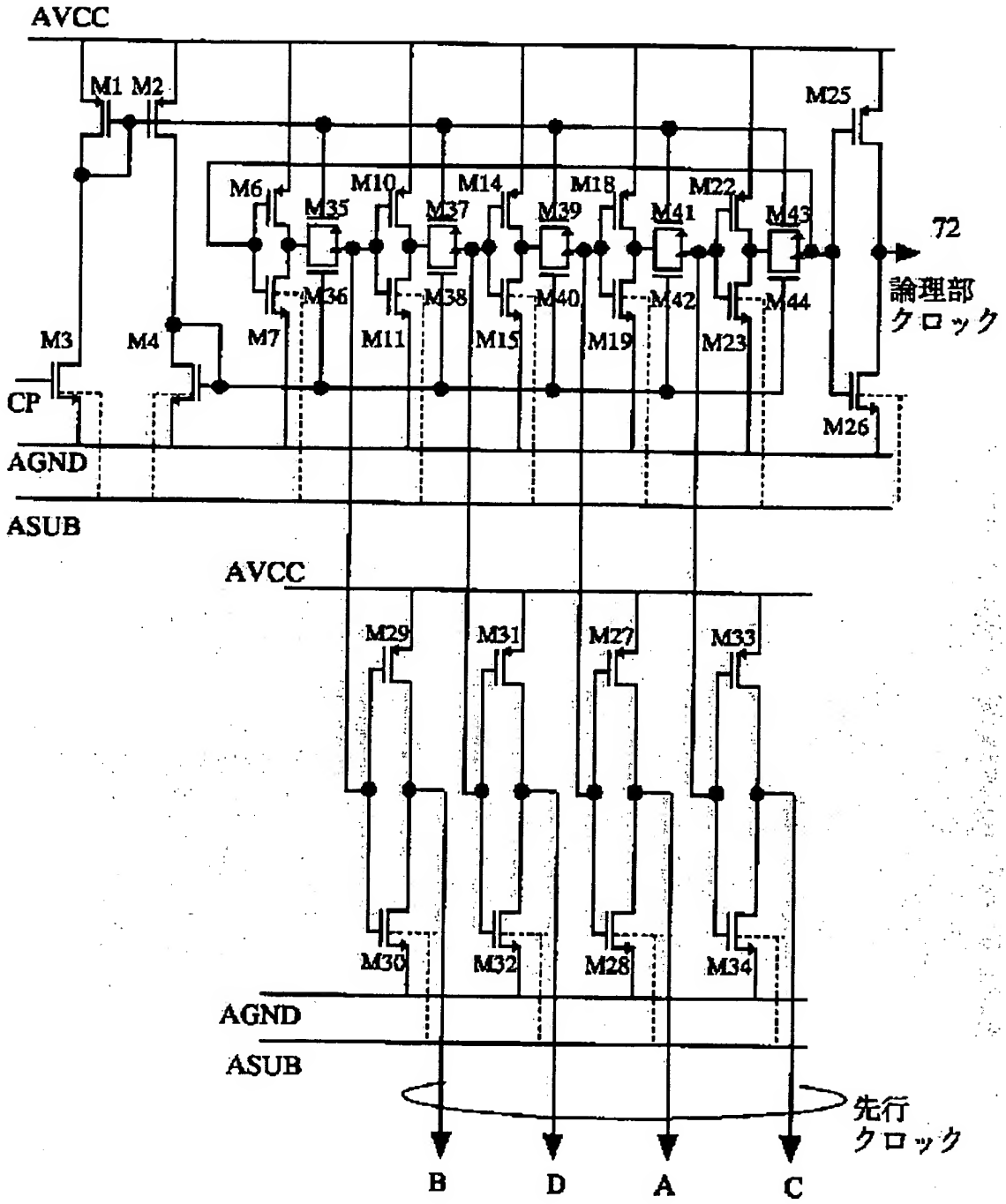
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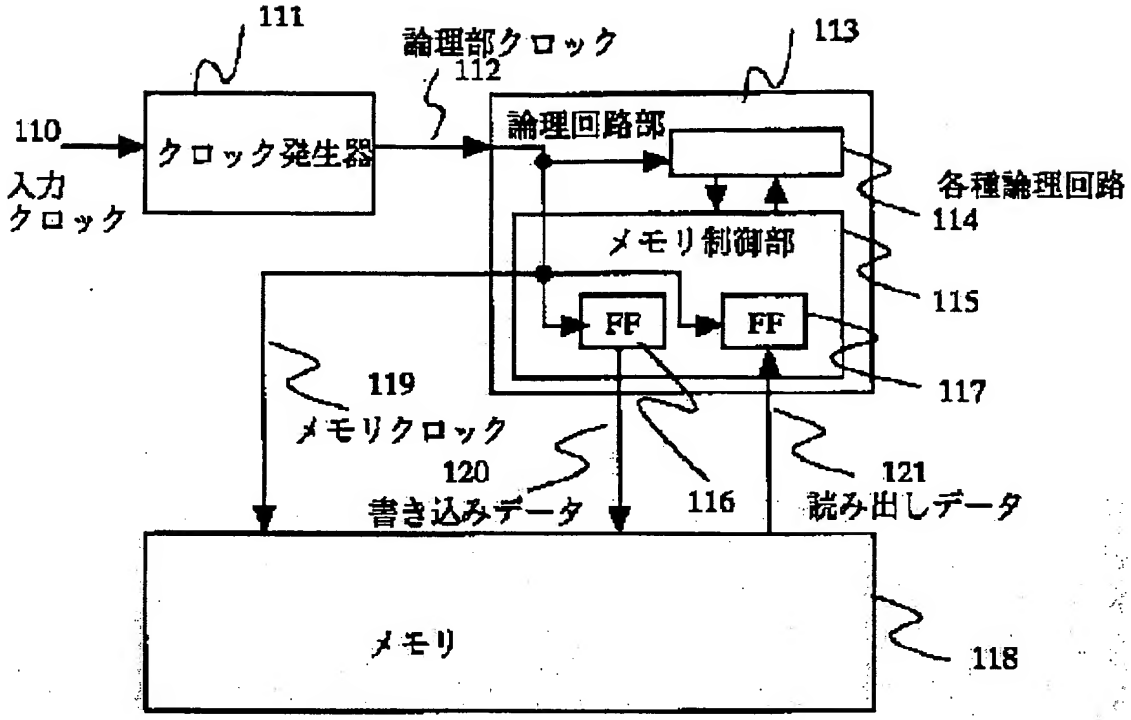
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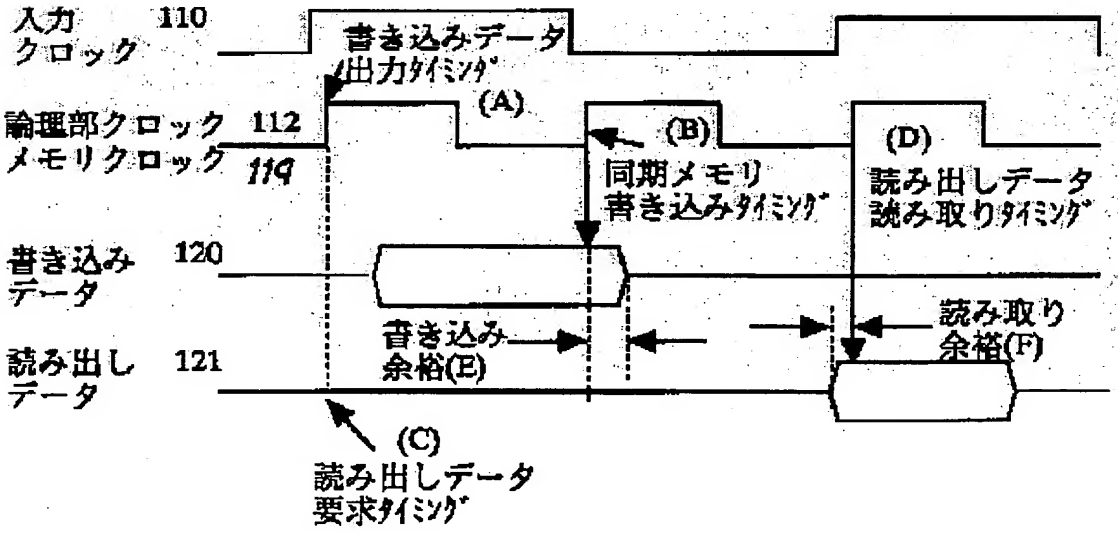
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